Low Surface-Field DMOS Structures for High-Voltage SiC Power MOS-Gated Bipolar Transistors with Trench Epitaxial Refill Technology

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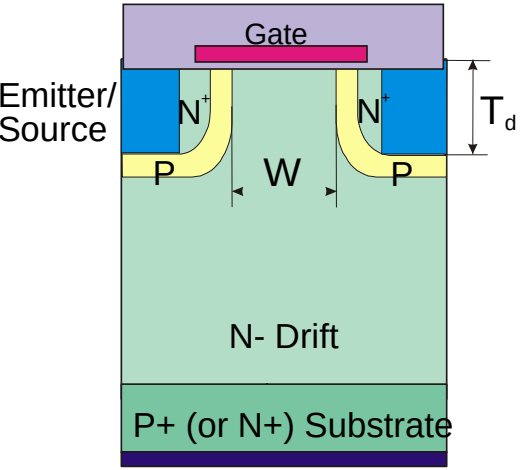

Collector/Drain

Hot-wall reactor

Objective: Demonstrate low surface-field high-voltage (up to 10kV) 4H-SiC DMOS power transistors with trench epitaxial refill technology

Technical Approach: Develop thick epitaxial growth process using a hotwall reactor

Evaluate PiN and DMOS process technologies using trench epitaxial refill

Optimize MOS properties using novel dielectric deposition and annealing processes

Study V_f drift in forward biased P-i-N diodes

Key Accomplishments

- Installed a vertical hot wall SiC epitaxial reactor and demonstrated growth of low doped ($<5x10^{14}cm^{-3}$) , thick (>50μm) 4H-SiC epitaxial layers.
- Demonstrated electrochemical polishing process for n-SiC that resulted in atomically smooth surface.
- Invented a new high temperature mask for the selective growth of SiC on SiC substrates.
- Invented a new simplified edge termination process for PiN rectifiers
- Completed two lots of high voltage PiN rectifiers with the new edge termination process
- Completed the design and fabrication of high voltage trench DMOS lot, and completed the mask with improved design

Major Impact of Technology

- Development of polishing process and growth of thick epitaxial films with reduced defect densities
- Trench refilling process using selective epitaxial regrowth to realize novel device structures
- Low surface-field DMOS power unipolar/bipolar transistors for improved ruggedness and reliability

Technology Transition Plan

- RPI inventions will be licensed to other contractors under DARPA WBG HPE program.
- The results will be presented in international conferences and published in archival journals.